WHAT IS CLAIMED IS:

1. A delta-sigma modulation system comprising:

an M-order filter to process input data, wherein M is greater than or equal to 3;

an N-order filter that is stable during overload conditions; and

a quantizer system coupled to the M-order and N-order filters to receive input data from the M-order and N-order filters, provide quantized feedback data, q_M, to the M-order filter, provide quantized feedback data, q_N, to the N-order filter, and provide two state quantization output data q, wherein $q = q_M + q_N$.

2. The delta-sigma modulation system of claim 1 wherein a maximum value of feedback data q_M is greater than a maximum value of output data q, and a minimum value of feedback data q_M is less than a minimum value of output data q.

3. The delta-sigma modulation system of claim 1 wherein q is an element of the logical value set [+1, -1], a maximum value of feedback data q_M is greater than +1, and a minimum value of feedback data q_M is less than -1.

4. The delta-sigma modulation system of claim 3 wherein feedback data q_M and q_N are integers.

5. The delta-sigma modulation system of claim 3 wherein feedback data q_M and q_N are real numbers including non-integers.

6. The delta-sigma modulation system of claim 1 wherein N equals 2.

7. The delta-sigma modulation system of claim 1 further wherein the input signal is a decimated version of a digital audio signal.

8. The delta-sigma modulation system of claim 1 wherein the input signal is a digital input signal.

9. A digital signal processing system having a delta-sigma modulator with stability protection during quantizer overload conditions, the system comprising:

an M-order loop filter to process a sum of input data and feedback data, q_M, wherein M is more than two;

an N-order loop filter to process feedback data, q_N, wherein N is selected from the group consisting of one and two;

a rules based 1-bit quantizer to process output data from the N-order loop filter and M-order filter and to provide q_M, q_N, and 1-bit quantized output data, q, wherein $q = q_M + q_N$, and q_{Mmax} is greater than the maximum value of q and q_{Mmin} is less than the minimum value of q to maintain stability of the M-order loop filter during overload conditions.

10. The digital signal processing system of claim 9 wherein overload conditions include conditions wherein a significant probability exists that input data to the quantizer will cause the M-order filter to become unstable if q_M does not exceed the maximum range of q.

11. A digital signal processing system comprising:

an M-order filter to process input data, wherein M is greater than 2;

an N-order filter that is stable during overload conditions; and

a quantizer system coupled to the M-order and N-order filters to receive input data from the M-order and N-order filters, provide quantized feedback data to the M-order filter, provide quantized feedback data to the N-order filter, and provide two state quantization output data, wherein the quantization output data approximately equals the feedback data to the M-order filter plus the feedback data to the N-order filter.

12. The digital signal processing system of claim 11 wherein a maximum value of feedback data is greater than a maximum value of output data, and a minimum value of feedback data is less than a minimum value of output data.

13. A method of maintaining stability of a 1-bit delta-sigma modulation system under overload conditions, the method comprising:

providing quantized output data using output data of an M-order filter and output data of an N-order filter, wherein M is greater than or equal to 3 and the N-order filter is stable under overload conditions;

providing feedback data, q_M, to the N-order filter;

providing feedback data q_N to the N-order filter; and

providing 1-bit quantization output data, q, wherein q equals $q_N + q_M$.

14. The method of claim 13 wherein a maximum value of feedback data q_M is greater than a maximum value of output data q, and a minimum value of feedback data q_M is less than a minimum value of output data q.

15. The method of claim 14 wherein feedback data q_M and q_N are integers.

16. The method of claim 14 wherein feedback data q_M and q_N are real numbers including non-integers.

17. The method of claim 13 wherein q is an element of the logical value set [+1, -1], a maximum value of feedback data q_M is greater than +1, and a minimum value of feedback data q_M is less than -1.

18. The method of claim 13 wherein N equals 2.

19. The method of claim 13 further wherein the input signal is an oversampled version of a digital audio signal.

20. The method of claim 13 further comprising:

receiving a digital input signal;

providing the digital input signal to the N-order filter; and

converting the 1-bit quantization output data into encoded audio data.

21. A method of maintaining stability of a 1-bit delta-sigma modulator during overload conditions, wherein the 1-bit delta-sigma modulator comprises a quantizer, an M-order loop filter, and an N-order loop filter, the method comprising:

providing 1-bit output data, q, based on input data from an M-order loop filter and an N-order loop filter, wherein M is greater than or equal to three and N is selected to provide stability to the delta-sigma modulator during overload conditions;

detecting an overload condition of a quantizer;

providing appropriate feedback data, q_M, for the M-order loop filter to enable the M-order loop filter to remain stable during the overload conditions, wherein a maximum value of feedback data q_M is greater than the maximum value of output data q; and

providing compensating feedback data, q_N, for the N-order loop filter to maintain an acceptable gain level of the quantizer.

22. The method of claim 21 further comprising:

determining q_M and q_N using a predetermined set of rules.

23. The method of claim 21 wherein $q = q_M + q_N$.